Amendments To The Claims

The following list of the claims replaces all prior versions and lists of the claims in this application.

Claims 1-29 (Canceled).

30. (Currently amended) A complimentary metal oxide semiconductor ~~(CMOS),~~ CMOS) device, featuring a P channel metal oxide semiconductor ~~(PMOS),~~ (PMOS) component in a first region of a semiconductor substrate, and featuring an N channel metal oxide semiconductor ~~(NMOS),~~ (NMOS) component in a second region of said semiconductor substrate, comprising:

a P well region located in a top portion of said ~~first~~ second region of said semiconductor substrate, and an N well region located in a top portion of said ~~second~~ first region of said semiconductor substrate;

an insulator filled, shallow trench isolation region, located in a top portion of said semiconductor substrate between said P well region and said N well region;

a recessed P well region located in the perimeter of said P well region, with a non-recessed P well portion of said semiconductor substrate located in the center of said P well region, surrounded by said recessed P well region;

a recessed N well region located in the perimeter of said N well region, with a non-recessed N well portion of said semiconductor substrate located in the center of said N well region, surrounded by said recessed N well region;

a heavily doped P type source/drain region, located in a top portion of said recessed ~~P well~~ N well region;

a heavily doped N type source/drain region, located in a top portion of said recessed ~~N well~~ P well region;

first metal silicide layers located in top portions of said heavily doped P type source/drain region, and second metal silicide layers located in top portions of said N type heavily doped source/drain region;

a first metal oxide gate insulator layer located overlying the top surface of said non-recessed P well portion of said semiconductor substrate, and a second metal oxide gate insulator layer overlying the top surface of said non-recessed N well portion of said semiconductor substrate;

vertical P type silicon spacers located on the sides of said non-recessed ~~P well~~ N well portion of said semiconductor substrate, and located on the sides of a bottom portion ~~of a~~ of said first metal oxide gate insulator layer;

vertical N type silicon spacers located on the sides of said non-recessed ~~N well~~ P well portion of said semiconductor substrate, and located on the sides of a bottom portion ~~of a~~ of said second metal oxide gate insulator layer;

conductive gate structures located overlying the metal oxide gate insulator layers;

an interlevel dielectric (ILD) layer located overlying said conductive gate structures;

contact hole openings in said ILD layer exposing top surface of said conductive gate structures, and exposing top surface of said heavily doped P type source/drain region, and of said heavily doped N type source/drain region; and

metal structures located in said contact hole openings.

31. (Currently amended) The CMOS device of claim 30, wherein the depth of said recessed P well region, located in the perimeter of said P well region, and of said recessed N well region, located in the perimeter of said N well region, is between about 100 to 100,000 Angstroms.

32. (Original) The CMOS device of claim 30, wherein said vertical P type silicon spacers, and said vertical N type silicon spacers, are comprised of polysilicon.

33. (Original) The CMOS device of claim 30, wherein said metal oxide gate insulator layers are comprised of either aluminum oxide (Al_2O_3), zirconium oxide (ZrO_2), or hafnium oxide (HfO_2), at a thickness between about 10 to 1000 Angstroms, and with said metal oxide gate insulator layers comprised with a dielectric constant between about 7 to 100.

34. (Original) The CMOS device of claim 30, wherein said conductive gate structures are comprised of either tungsten, aluminum, aluminum-copper, copper, tungsten silicide, or doped polysilicon.

35. (Original) A metal oxide semiconductor field effect transistor (MOSFET) device, comprising:

a well region located in a top portion of a semiconductor substrate;

a recessed well region located in the perimeter of said well region, with a non-recessed well portion of said semiconductor substrate located in the center of said well region, surrounded by said recessed well region;

a heavily doped source/drain region located in a top portion of said recessed well region;

metal silicide layers located in top portions of said heavily doped source/drain region;

a metal oxide gate insulator layer located overlying the top surface of said non-recessed well portion of said semiconductor substrate;

vertical silicon spacers located on the sides of said non-recessed well portion of said semiconductor substrate, and located on the sides of a bottom portion of said metal oxide gate insulator layer;

a conductive gate structure located overlying said metal oxide gate insulator layer;

an interlevel dielectric (ILD) layer located overlying said conductive gate structure;

contact hole openings in said ILD layer exposing top surface of said conductive gate structure, and exposing top surface of said heavily doped source/drain region; and

metal structures located in said contact hole openings.

36. (Original) The MOSFET device of claim 35, wherein said well region is a P type well region.

37. (Original) The MOSFET device of claim 35, wherein said well region is an N type well region.

38. (Currently amended) The MOSFET device of claim 35, wherein the depth of said recessed well region, located in the perimeter of said well region, is between about 100 to 100,000 Angstroms.

39. (Original) The MOSFET device of claim 35, wherein said vertical silicon spacers are comprised of either P type doped polysilicon or of N type doped polysilicon.

40. (Original) The MOSFET device of claim 35, wherein said metal oxide gate insulator layer is comprised of either aluminum oxide (Al_2O_3), zirconium oxide (ZrO_2), or hafnium oxide (HfO_2), at a thickness between about 10 to 1000 Angstroms, and with said metal oxide gate insulator layer comprised with a dielectric constant between about 7 to 100.

41. (Original) The MOSFET device of claim 35, wherein said conductive gate structure is comprised of either tungsten, aluminum, aluminum-copper, copper, tungsten silicide, or doped polysilicon.